ABSTRACT

A semiconductor device (1) includes an n-type silicon carbide substrate (2) of a high impurity concentration, an n-type silicon carbide layer (3) of a low impurity concentration disposed on the substrate, a first n-type silicon carbide region (4) of a first impurity concentration disposed on the surface of the n-type silicon carbide layer, first p-type silicon carbide regions (5) disposed as adjoined to the opposite sides of the first n-type silicon carbide region, a second n-type silicon carbide region (6) disposed selectively from the surface through the interior of the first p-type silicon carbide region, polycrystalline silicon (7) short-circuiting the first p-type silicon carbide region (5) to the second n-type silicon carbide region (6), a gate electrode (8) and a third n-type silicon carbide region (10), wherein the components thereof are individually constructed in a vertical DMOS structure. Since the polycrystalline silicon short-circuits the first p-type silicon carbide region to the second n-type silicon carbide region, the threshold voltage can be given a fixed value, and the device can be used as an actual MISFET.